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10/044,295	01/11/2002	Shigetsugu Okamoto	70904/56,851	6848

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EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2673	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/044,295	Applicant(s) OKAMOTO, SHIGETSUGU	
	Examiner Nitin Patel	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 16* is/are rejected.

7)☒ Claim(s) *7-15 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the output of the inverter which function as an output end of the memory element is directly connected to one of end of the optical modulation element (12) which is not shown in fig.1, in fact the output of the inverter is directly connected to a input of the inverter (element p1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Prache (US20020044110 A1).

As per claim 1, AAPA shows memory-integrated display element (In Fig.21), comprising: an optical modulation element (element 112 In Fig.21) provided in a pixel

(element 104b In fig.21); a memory element, provided in the pixel, which stores binary data, which indicates a value inputted to the optical modulation element 9In Fig.21).

AAPA does not show said memory element is arranged by connecting at least two inverters to each other in a loop manner, and an output of an output inverter, one of the inverters, which functions as an output end of the memory element, is directly connected to one end of the optical modulation element.

Prache shows memory element (element 72,74,76 In Fig.3 and In section 0022) is arranged by connecting at least two inverters to each other in a loop manner (Q1-Q4), and an output of an output inverter, one of the inverters, which functions as an output end of the memory element, is directly connected to one end of the optical modulation element (OLED D1 In Fig.3 and section 0022). It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to allow the teaching of Prache's loop inverter into pixel circuit of AAPA's because it would have controlled input of the corresponding current driver to control the grayscale current provided to the OLED.

As per claim 2, AAPA shows memory-integrated display element wherein said optical modulation element ((element 112 in Fig.21) is a current drive type optical modulation element whose luminous intensity varies in accordance with a current quantity (In specification paragraph 1).

As per claim 3, AAPA shows said optical modulation element is an Organic Light Emission Diode (element 112 In Fig.21).

As per claim 4, AAPA shows memory-integrated display element further comprising electric charge emitting means for emitting electric charge, which has been stored in the optical modulation element while the memory element was applying a voltage to the optical modulation element, after the memory element finishes applying the voltage (In specification on page 27 last paragraph).

As per claim 5,6 AAPA does not show the memory-integrated display element output inverter is a complementary inverter and the memory-integrated display element set wherein said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line.

Prache shows the memory-integrated display element output inverter is a complementary inverter (in Fig.3) and the memory-integrated display element (element 72,74,76) wherein said complementary inverter includes: a p type transistor connected to a first power line (Vcc in fig.3); and an n type transistor connected to a second power line (Van In fig.3), and an anode of the optical modulation element is connected to an output end of the output inverter (In Fig.3), and a cathode of the optical modulation element is connected to the second power line(In Fig.3). It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to allow the teaching of Prache's loop inverter into pixel circuit of AAPA's because it would have

controlled input of the corresponding current driver to control the grayscale current provided to the OLED.

As per claim 16, AAPA shows memory-integrated display element, wherein said optical modulation element and said memory element are included in each of plural sub pixels, which make up one pixel unit (In Fig.21 element 111 as sub pixel).

Allowable Subject Matter

4. Claims 7-15,17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach or suggest memory-integrated display element wherein said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line, and when a ratio of an OFF resistance value of the n type transistor with respect to an ON resistance value of the p type transistor is K, a ratio of an ON resistance value of the p type transistor with respect to an ON resistance value of the optical modulation element is set to be substantially (K+1).sup.1/2/K as claimed in claim 7.

Response to Arguments

5. Applicant's arguments with respect to claims1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 703-308-7024. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP

VIJAY SHANKAR
PRIMARY EXAMINER